

Confirmation No. 3317

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Detechevery, Celine	Examiner:	Baisa, Joselito
Serial No.:	10/564,582	Group Art Unit:	2832
Filed:	January 12, 2006	Docket No.:	NL030878US
Title:	INDUCTIVE AND CAPACITIVE ELEMENTS FOR SEMICONDUCTOR TECHNOLOGIES WITH MINIMUM PATTERN DENSITY REQUIREMENTS		

APPEAL BRIEF

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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed August 7, 2008 and in response to the rejections of claims 1-22 as set forth in the Final Office Action dated May 27, 2008 and in further response to the Advisory Action dated July 24, 2008.

Please charge Deposit Account number 50-0996 (NXPS.267PA) \$540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 019719/0843 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-22 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Office Action dated January 18, 2008.

V. Summary of Claimed Subject Matter

The claimed invention is directed to an important advancement involving the use of tilling structures in a semiconductor device that includes an inductor. Appellant's tilling structures are electrically connected together and arranged in a geometrical pattern that substantially inhibits an inducement of an image current in the tilling structures that is caused by a current in the inductor. Appellant recognized that using tilling structures with specific geometrical arrangements relative to the inductor prevents the inducement of an image current in the tilling structures and thus enabling the use of such tilling structures in a device with an inductor. *See, e.g.*, Appellant's Figures 3-5 and 7-9. Tilling structures (as is known in the art) are used to increase or decrease the pattern density in empty or large metal areas, respectively, of a semiconductor device. *See, e.g.*, Page 1:21-28 of Appellant's Specification and U.S. Patent No. 7,152,215, Col. 1:54-59. Tilling structures improve manufacturability of the semiconductor device, for example, by improving planarity, by improving the integrity of dielectric material, and/or by

improving the uniformity of the removal rate of Chemical Mechanical Polishing. In the discussion below, the claims are directed to semiconductor devices that includes an inductor and tilling structures.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a semiconductor device comprising a plurality of layers (*see, e.g.*, device 10 shown in Figs. 1 and 2, and page 8:5-19). The semiconductor device includes a substrate (*see, e.g.*, substrate 20 shown in Fig. 2, and page 8:14-15) having a first major surface and an inductive element (*see, e.g.*, element 11 shown in Fig. 1, and page 8:6-7) fabricated on the first major surface of the substrate the inductive element comprising at least one conductive line. The semiconductor device further includes a plurality of tilling structures in at least one layer (*see, e.g.*, metal stripes 12 and pattern 14 shown in Fig. 1, and page 8:10-12), the plurality of tilling structures arranged to improve manufacturability of the semiconductor device (*see, e.g.*, page 1:21-29), wherein the plurality of tilling structures are electrically connected together and arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element (*see, e.g.*, page 8:16 to page 9:11).

Commensurate with independent claim 22, an example embodiment of the present invention is directed to a method for providing an inductive element in a semiconductor device comprising a plurality of layers (*see, e.g.*, device 10 shown in Figs. 1 and 2, and page 8:5-19). The method includes providing a substrate having a first major surface (*see, e.g.*, substrate 20 shown in Fig. 2, and page 8:14-15), forming an inductive element (*see, e.g.*, element 11 shown in Fig. 1, and page 8:6-7) above the first major surface of the substrate, the inductive element comprising at least one conductive line, providing a plurality of tilling structures (*see, e.g.*, metal stripes 12 and pattern 14 shown in Fig. 1, and page 8:10-12) in at least one layer to improve manufacturability of the semiconductor device (*see, e.g.*, page 1:21-29), wherein the plurality of tilling structures are electrically connected together and are arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element (*see, e.g.*, page 8:16 to page 9:11).

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein.

Appellant notes that representative subject matter is identified for these claims; however,

the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection to be Reviewed Upon Appeal

Claims 1-22 stand rejected under 35 U.S.C. § 103(a) over Hiromoto (JP2001230375A).

VII. Argument

The rejection of claims 1-22 under U.S.C. § 103(a) over Hiromoto should be reversed because Hiromoto fails to disclose each recited claim limitation.

The claimed invention is directed to an important advancement that enables tilling structures to be used in a semiconductor device that includes an inductor. Appellant recognized that using tilling structures with specific geometrical arrangements relative to the inductor prevents the inducement of an image current in the tilling structures that is caused by current flowing through the inductor. As a result, Appellant's tilling structures can be used in semiconductor devices that include an inductor thereby improving manufacturability of such semiconductor devices. *See, e.g.*, Appellant's Figures 3-5 and 7-9 and Page 1:21-28 of Appellant's Specification.

The § 103 rejection must be reversed because each and every recited claim element is not taught by the asserted combination of teachings. As discussed under Section A, *supra*, the record is uncontroverted that the Examiner fails to address aspects of the claimed invention directed to the arrangement of Appellant's tilling structures. In the alternative, the Examiner erroneously argues that the inherent function of a tilling structure (*i.e.*, to improve manufacturability of the device) is a product by process limitation and therefore permitting the Examiner to ignore these aspects. As is discussed under the remaining Sections (B, C, D and E), the Hiromoto reference further fails to

teach or suggest numerous other aspects of the claimed invention; for example, Hiromoto fails to teach tilling structures, Hiromoto fails to teach several additional aspects relating to Appellant's tilling structures, and Hiromoto fails to teach a further passive element. A detailed discussion of the specific differences between the subject matter of the claims and the asserted Hiromoto reference follows.

A. The rejection of claims 1-22 under U.S.C. § 103(a) over Hiromoto should be reversed because the Examiner improperly fails to address aspects of the claimed invention directed to the arrangement of the tilling structures.

The § 103(a) rejection of claims 1-22 must be reversed because the Examiner improperly fails to address aspects of the claimed invention directed to tilling structures that are arranged to improve manufacturability of the semiconductor device. Instead, the Examiner erroneously asserts that aspects relating to how Appellant's tilling structures are arranged are product by process limitations. *See, e.g.*, page 7 of the final Office Action dated 5/27/08. Appellant submits that this position is disingenuous because claim 1 does not include any steps or process limitations. According to M.P.E.P. § 2173.05(p), a product by process claim is a product claim that defines the claimed product in terms of the process by which it is made. In this instance, the claimed aspects relating to the tilling structures are directed to the tilling structures themselves, not the process by which the tilling structures or any other elements are made.

The following are specific examples of structural limitations of Appellant's tilling structures that have been ignored by the Examiner. As a first example, claim 1 includes aspects directed to the tilling structure arrangement (*e.g.*, the tilling structures are arranged to improve manufacturability of the semiconductor device). Appellant's disclosure includes numerous examples of tilling structures that improve manufacturability of the semiconductor device and that prevent inducement of an image current in the tilling structures (*see, e.g.*, Appellant's Figures 3-5 and 7-9). As a second example, claim 2 recites that the structure of the tilling structures is such that the amount of tilling structure material present in the area near the inductive element is smaller than the amount of tilling structure material present in the area farther away from the inductive element. As a third example, claim 3 includes aspects directed to how the structural

arrangement of the tilling structures is determined. Thus, these aspects related to the arrangement of the tilling structures are structural limitations that must be addressed by the Examiner.

In addition, Appellant notes that claim 22 is a method claim (*i.e.*, a process); as such, any assertion regarding product by process limitations is inapplicable to claim 22. Thus, the Examiner has failed to present any basis for the rejection of claim 22.

For at least the reasons presented above, Appellant submits that the § 103(a) rejection of claims 1-22 fails, and therefore must be reversed.

B. The rejection of claims 1-22 under U.S.C. § 103(a) over Hiromoto should be reversed because Hiromoto fails to disclose a plurality of tilling structures.

The § 103(a) rejection of claims 1-22 must be reversed because Hiromoto fails to teach Appellant's claimed features relating to a plurality of tilling structures, which are inherently arranged to improve manufacturability of the semiconductor device. The Examiner misconstrues the cited portions of Hiromoto as corresponding to Appellant's tilling structures. According to M.P.E.P. § 2111.01, the words of the claim cannot be interpreted in a manner that is inconsistent with the Appellant's specification.

In this instance, the Examiner's contention that Hiromoto's ground shield corresponds to the claimed tilling structures is inconsistent with the meaning of a tilling structure as defined by Appellant's specification. The record is uncontroverted that the cited portions of Hiromoto teach a ground shield and not tilling structures (*see e.g.*, Figure 3a of Hiromoto, Appellant's Figure 2 and Paragraphs 0063-0065 of Appellant's Specification); specifically, Hiromoto teaches that polysilicon 5b and metal silicide 8b form the 1st shielding pattern, which together with the 2nd shielding pattern (*i.e.*, metal silicide 8d) form a ground shield layer. *See, e.g.*, Figure 3a and paragraphs 0012, 0014 and 0036. Appellant submits that the skilled artisan would recognize that Hiromoto's ground shield does not correspond to the tilling structures of the claimed invention. *See, e.g.*, Page 1:21-28 of Appellant's Specification. More specifically, Appellant's specification states that tilling structures (as is known in the art) are used to increase or decrease the pattern density in empty or large metal layers respectively in order to improve the manufacturability of the semiconductor device. *See, also*, U.S. Patent No.

7,152,215, Col. 1:54-59. In contrast, Hiromoto's ground shield layer is used to prevent coupling between an inductor and a substrate. *See, e.g.*, Figure 3a of Hiromoto, Appellant's Figure 2 and Paragraphs 0063-0065 of Appellant's Specification. As such, Hiromoto's ground shield layer is not taught to increase or decrease the pattern density for manufacturability. Accordingly, Appellant submits that the Examiner's assertion that Hiromoto's ground shield corresponds to Appellant's tilling structures is inconsistent with the meaning of a tilling structure as defined by Appellant's specification, which differentiates a ground shield from tilling structures. Thus, the cited portions of Hiromoto do not correspond to the claimed invention.

Moreover, certain embodiments of the claimed invention (*see, e.g.*, 11-13) include a ground shield. In attempting to address these aspects, the Examiner highlights the impropriety of asserting that Hiromoto's ground shield corresponds to Appellant's tilling structures because the Examiner asserts that part of Hiromoto's ground shield layer (*i.e.*, metal silicide 8d) corresponds to Appellant's ground shield. *See, e.g.*, page 5 of the final Office Action.

For at least the reasons presented above, Appellant submits that the § 103(a) rejection of claims 1-22 fails, and therefore must be reversed.

C. The rejection of claim 4 under U.S.C. § 103(a) over Hiromoto should be reversed because Hiromoto fails to disclose tilling structures that are different in shape and/or orientation.

The § 103(a) rejection of claim 4 must be reversed because Hiromoto does not teach that the geometrical pattern of the tilling structures at two different layers is different in shape and/or orientation. The Examiner improperly asserts that Hiromoto's polysilicon 5b and metallic silicate 8b (*i.e.*, the Examiner's alleged tilling structures) are different in shape and/or orientation. *See, e.g.*, Figure 1a. The cited portions of Hiromoto teach that polysilicon 5b and metallic silicate 8b each have the same shape and orientation (*i.e.*, metallic silicate 8b is formed on top of polysilicon 5b), with polysilicon 5b and metallic silicate 8b forming the 1st shielding pattern. *See, e.g.*, Figures 1b and 3; and paragraph 0012.

The Examiner improperly relies upon Hiromoto's Figure 1a to assert that polysilicon 5b and metallic silicate 8b are of different shape and orientation. *See, e.g.*,

page 8 of the final Office Action dated 5/27/08. However, Hiromoto's Figure 1a mislabels those parts that are identified as 8b. The parts of Figure 1 that are labeled 8b are actually the second shielding pattern 8d. Specifically, Hiromoto discusses in paragraph 0013 that metal silicide 8d contains connection field 8d-2 that extends into the slitting 15 (formed in polish recon 5b) and that connection field 8d-2 connects with metal silicide 8d-1. Hiromoto's Figure 1b shows that metal silicide 8b is located on top of polish recon 5b, and Hiromoto's Figure 3a shows that metal silicide 8d extends into the slitting 15 in metal silicide 8b. Thus, Hiromoto teaches that polysilicon 5b and metallic silicate 8b each have the same shape and orientation. Appellant submits that Hiromoto's Figure 1a mislabels regions 8d as 8b; as such, Figure 1a in view of the remainder of the Hiromoto reference does not support the Examiner's assertion that polysilicon 5b and metallic silicate 8b (*i.e.*, the Examiner's alleged tiling structures) are different in shape and/or orientation.

For at least the reasons presented above, Appellant submits that the § 103(a) rejection of claim 4 fails, and therefore must be reversed.

D. The rejection of claims 8 and 10 under U.S.C. § 103(a) over Hiromoto should be reversed because Hiromoto fails to disclose tiling structures that are a plurality of substantially triangular elements.

The § 103(a) rejection of claims 8 and 10 must be reversed because the Hiromoto reference does not teach that polysilicon 5b and metallic silicate 8b (*i.e.*, the Examiner's alleged tiling structures) are formed of substantially triangular elements. *See, e.g.*, Figures 1a, 1b and 3. The Examiner cites to the square corners of polysilicon 5b and the Examiner asserts that each of these squares is formed of two triangular elements if one were to draw a line bisecting the square. *See, e.g.*, pages 8-9 of the final Office Action dated 5/27/08. Appellant submits that the Examiner's interpretation essentially gives no meaning to the tiling structures being a plurality of substantially triangular elements (*i.e.*, the Examiner is improperly reading these aspects out of the claim by asserting that correspondence can be shown by citation to a square). *See, e.g.*, M.P.E.P. § 2111.01. Such an interpretation would allow the Examiner to arbitrarily draw lines through any shape to arrive at triangles. In other words, following the Examiner's logic, correspondence to a circle could be shown by citing to a square and drawing a line in the

square to form a circle. The Examiner's approach goes beyond a reasonable interpretation as it essentially gives no meaning to such claim limitations. A proper interpretation would be that the cited portions of Hiromoto (*i.e.*, the square corners of polysilicon 5b) are formed of squares instead of a plurality of substantially triangular elements as are the tiling structures of the claimed invention.

For at least the reasons presented above, Appellant submits that the § 103(a) rejection of claims 8 and 10 fails, and therefore must be reversed.

E. The rejection of claims 15-21 under U.S.C. § 103(a) over Hiromoto should be reversed because Hiromoto fails to disclose a further passive element.

The § 103(a) rejection of claims 15-21 must be reversed because the Hiromoto reference fail to even mention a further passive element, let alone that the further passive element is a capacitor (*e.g.* claim 16). *See, e.g.*, Figure 3, paragraph 0036, and the Abstract. Specifically, these portions of Hiromoto discuss the parasitic capacitance between the inductor and the 1st and 2nd shield patterns, not that the device includes a separate passive element (*e.g.*, a capacitor). Appellant submits that the skilled artisan would readily recognize that a parasitic capacitance is not equivalent to a separate capacitive element.

The Examiner further (erroneously) asserts that it would be obvious to the skilled artisan "to produce a passive element, *i.e.*, capacitor, (if needed in the circuit) since the structure of Hiromoto discloses capacitive properties being present in its structure." *See, e.g.*, page 9 of the final Office Action dated 5/27/08. Thus, the Examiner appears to be taking Official Notice that it would be obvious to combine a capacitor with Hiromoto; however, according to M.P.E.P. § 2144.03, "It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known." The Examiner presented this apparent reliance upon Official Notice for the first time in the final Office Action. Appellant responded by indicating why such reliance upon Official Notice was improper. *See, e.g.*, page 9 of the Response dated July 10, 2008. Specifically, the various aspects of claims 15-21 are not capable of instant and unquestionable demonstration as being well-known, since Hiromoto does not even

disclose a separate capacitive element. The Examiner, in the Advisory Action dated July 24, 2008, failed to provide the required documentary evidence to support any such reliance upon Office Action. Thus, the Examiner's apparent reliance upon Official Notice is improper due to the lack of citation to a prior art reference to support the use of Official Notice.

Moreover, the Examiner improperly concludes that the skilled artisan would combine a capacitor with Hiromoto without providing any reason why the skilled artisan would combine these elements. *See, e.g.*, M.P.E.P. § 2141 ("rejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."), *see also KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007) ("A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art.") Appellant submits that the Examiner's assertion that a capacitor could be combined with Hiromoto "if needed in the circuit" highlights the fact that the Examiner has not identified a reason to modify Hiromoto (*i.e.*, why a capacitor is needed). Thus, the Examiner has failed to provide any reason why the skilled artisan would combine a capacitor with Hiromoto in direct contradiction of the requirements of § 103 and relevant law.

In addition, Appellant notes that a purpose of the Hiromoto reference is to reduce the above discussed parasitic capacitance. *See, e.g.*, paragraph 0036. Thus, Appellant submits that Hiromoto appears to teach away from adding a separate capacitive element. *See, e.g.*, M.P.E.P. § 2141.02.

For at least the reasons presented above, Appellant submits that the § 103(a) rejection of claims 15-21 fails, and therefore must be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-22 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/564,582)

1. A semiconductor device comprising a plurality of layers, the semiconductor device comprising:
 - a substrate having a first major surface,
 - an inductive element fabricated on the first major surface of the substratethe inductive element comprising at least one conductive line,
 - a plurality of tilling structures in at least one layer, the plurality of tilling structures arranged to improve manufacturability of the semiconductor device,wherein the plurality of tilling structures are electrically connected together and arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element.
2. A semiconductor device according to claim 1, the tilling structures being made from tilling structure material, wherein the plurality of tilling structures are arranged in a pattern so that the amount of tilling structure material in an area closer to the inductive element is smaller than the amount of tilling structure material in an area farther away from the inductive element.
3. A semiconductor device according to claim 1, wherein the tilling structures are located at different layers, tilling structures at each layer being arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element, and wherein the arrangement of the tilling structures is determined by a desired pattern density of the semiconductor device for improving at least one of a process window of lithography, uniformity of Chemical Mechanical Polishing removal rate and integrity of low-k dielectrics.
4. A semiconductor device according to claim 3, wherein the geometrical pattern of tilling structures at two different layers is different in shape and/or orientation.

5. A semiconductor device according to claim 3, wherein the tilling structures at different layers are electrically connected to each other.
6. A semiconductor device according to claim 1, wherein the tilling structures are connected to a DC potential.
7. A semiconductor device according to claim 1, wherein the tilling structures are a plurality of slender elongate elements.
8. A semiconductor device according to claim 1, wherein the tilling structures are a plurality of substantially triangular elements.
9. A semiconductor device according to claim 7, wherein the elements of the tilling structures are locally oriented perpendicular to the at least one conductive line of the inductive element.
10. A semiconductor device according to claim 8, wherein the elements of the tilling structures are locally oriented perpendicular to the at least one conductive line of the inductive element.
11. A semiconductor device according to claim 1, furthermore comprising a ground shield for shielding the inductive element from a further layer.
12. A semiconductor device according to claim 11, wherein the further layer is the substrate.
13. A semiconductor device according to claim 11, furthermore comprising connection means electrically connecting the plurality of tilling structures with the ground shield without creating a conductive loop.
14. A semiconductor device according to claim 1, wherein the tilling structures are formed in a region other than a region directly below the inductive element.

15. A semiconductor device according to claim 1, furthermore provided with a further passive element.

16. A semiconductor device according to claim 15, wherein the further passive element is a capacitive element.

17. A semiconductor device according to claim 16, wherein the capacitive element comprises two capacitor electrodes at least one of the capacitor electrodes being formed by a plurality of tilling structures.

18. A semiconductor device according to claim 17, wherein a capacitor electrode formed by a plurality of tilling structures leads to a metal or polysilicon or active region density in the inductor vicinity respecting the design rules of advanced IC technologies.

19. A semiconductor device according to claim 17, wherein one capacitor electrode of the capacitive element is formed by a ground shield.

20. A semiconductor device according to claim 15, wherein the integration of the capacitive element with the inductive element is optimized to respect the metal pattern density in advanced silicon technologies.

21. A semiconductor device according to claim 15, wherein the distance between the capacitive element and the inductive element is large enough to avoid a dominant fringe coupling between them.

22. A method for providing an inductive element in a semiconductor device comprising a plurality of layers, the method comprising:

- providing a substrate having a first major surface,
- forming an inductive element above the first major surface of the substrate, the inductive element comprising at least one conductive line,

- providing a plurality of tilling structures in at least one layer to improve manufacturability of the semiconductor device,

wherein the plurality of tilling structures are electrically connected together and are arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.